

CLAIMS

What is claimed is:

1 1. A resistor comprising an ion implanted resistor
2 formed in a crystalline silicon substrate of the opposite
3 conductivity type, the resistor being isolated from the rest
4 of the substrate by a PN junction and having an implantation
5 dose providing a minimum resistance at a temperature of
6 approximately room temperature.

1 2. The resistor of claim 1 wherein the silicon
2 substrate is a p-type substrate and the resistor body is
3 formed by arsenic implantation.

1 3. The resistor of claim 1 wherein the temperature
2 variation of the resistance of the resistor across the
3 temperature range of -40C to +85C is less than 3%.

1 4. The resistor of claim 1 further comprising first
2 and second heavily doped regions of the same conductivity
3 type as the resistor body providing first and second contacts
4 to the resistor.

1 5. The resistor of claim 4 further comprising an
2 insulating layer over the resistor with contact openings
3 therein to provide access to the first and second heavily

4 doped regions, and a patterned metal layer there over
5 providing electrical contact to the heavily doped regions.

1 6. The resistor of claim 1 wherein the resistor
2 comprises part of a CMOS integrated circuit.

1 7. The resistor of claim 1 wherein the resistor
2 comprises part of a bipolar integrated circuit.

1 8. An integrated circuit on a crystalline silicon
2 substrate of a first conductivity type for operating over a
3 temperature range of T_1 to T_2 , including an ion implanted
4 resistor formed in the crystalline silicon substrate of the
5 opposite conductivity type, the resistor being isolated from
6 the rest of the substrate by a PN junction and having an
7 implantation dose providing a minimum resistance at a
8 temperature of approximately $(T_1 + T_2)/2$.

1 9. The integrated circuit of claim 8 wherein the
2 silicon substrate is a p-type substrate and the resistor body
3 is formed by arsenic implantation.

1 10. The integrated circuit of claim 9 wherein the
2 temperature T_1 is -40°C and T_2 is $+85^\circ\text{C}$.

1 11. The integrated circuit of claim 8 further
2 comprising first and second heavily doped regions of the same

3 conductivity type as the resistor body providing first and
4 second contacts to the resistor.

1 12. The integrated circuit of claim 11 further
2 comprising an insulating layer over the resistor with contact
3 openings therein to provide access to the first and second
4 heavily doped regions, and a patterned metal layer there over
5 providing electrical contact to the heavily doped regions.

1 13. The integrated circuit of claim 8 wherein the
2 integrated circuit is a CMOS integrated circuit.

1 14. The integrated circuit of claim 8 wherein the
2 integrated circuit comprises a bipolar integrated circuit.

1 15. The integrated circuit of claim 8 wherein the
2 minimum resistance is within 20C of the temperature of $(T_1 +$
3 $T_2)/2$.

1 16. The integrated circuit of claim 8 wherein the
2 minimum resistance is within 10C of the temperature of $(T_1 +$
3 $T_2)/2$.

1 17. The integrated circuit of claim 8 wherein the
2 minimum resistance is within 5C of the temperature of $(T_1 +$
3 $T_2)/2$.

1 18. The integrated circuit of claim 8 wherein the
2 resistances of the resistor at the two temperature extremes
3 are within 1% of each other.

1 19. The integrated circuit of claim 8 wherein the
2 resistances of the resistor at the two temperature extremes
3 are within 0.5% of each other.

1 20. The integrated circuit of claim 8 wherein the
2 resistances of the resistor at the two temperature extremes
3 are within 0.25% of each other.

1 21. A method of forming a resistor on a crystalline
2 silicon substrate in an integrated circuit intended to
3 operate over a temperature range of T_1 to T_2 comprising:
4 before a final high temperature exposure associated with
5 the processing of the active devices of the integrated
6 circuit, forming a resistor of one conductivity type in the
7 crystalline silicon substrate of an opposite conductivity
8 type by ion implantation, the resistor being isolated from
9 the rest of the substrate by a PN junction, using an
10 implantation dose providing, in the completed integrated
11 circuit, a minimum resistance at a temperature of
12 approximately $(T_1 + T_2)/2$.

1 22. The method of claim 21 wherein the silicon
2 substrate is a p-type substrate and the resistor body is
3 formed by arsenic implantation.

1 23. The method of claim 22 wherein the temperature T_1
2 is -40°C and T_2 is $+85^{\circ}\text{C}$.

1 24. The method of claim 22 further comprising forming
2 first and second heavily doped regions of the same
3 conductivity type as the resistor body to provide first and
4 second contacts to the resistor.

1 25. The method of claim 24 further comprising forming
2 an insulating layer over the resistor with contact openings
3 therein to provide access to the first and second heavily
4 doped regions, and providing a patterned metal layer there
5 over to provide electrical contact to the heavily doped
6 regions.

1 26. The method of claim 21 wherein the integrated
2 circuit is a CMOS integrated circuit.

1 27. The method of claim 21 wherein the integrated
2 circuit comprises a bipolar integrated circuit.

1 28. The method of claim 21 wherein the minimum
2 resistance is within 20C of the temperature of $(T_1 + T_2)/2$.

1 29. The method of claim 21 wherein the minimum
2 resistance is within 10C of the temperature of $(T_1 + T_2)/2$.

1 30. The method of claim 21 wherein the minimum
2 resistance is within 5C of the temperature of $(T_1 + T_2)/2$.

1 31. The method of claim 21 wherein the resistance
2 values of the resistor at the two temperature extremes are
3 within 1% of each other.

1 32. The method of claim 21 wherein the resistance
2 values of the resistor at the two temperature extremes are
3 within 0.5% of each other.

1 33. The method of claim 21 wherein the resistance
2 values of the resistor at the two temperature extremes are
3 within 0.25% of each other.